Hardware Implementation of FAST and Betweenness algorithms based on HLS

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On board test by Alveo U50

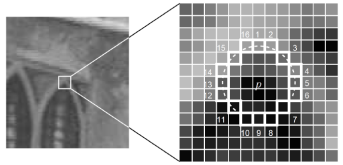
OpenHW2022

AMD XILINX

FAST

INTRODUCTION

FAST (Features from accelerated segment test) is a **corner point detection method**, which can be used to extract feature points and complete tracking and mapping objects. It is faster than other well-known feature point extraction methods such as SIFT, SUSAN, Harris. FAST corner detection method is very suitable for real-time video processing.

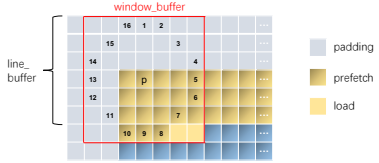


Corner point detection method

CREATIVE DESIGN

Use **#PRAGMA HLS DATAFLOW** to automate global function pipeline, means read the pixel value of the latter point while calculating. Using **on-chip cache and prefetch** to optimize **read_block module** outputing one data per cycle. Implement FIFO with **hls::stream** to keep data synchronized between multiple function modules. Each **7*7 convolution block** is packed into one piece of data in the FIFO.

Global dataflow scenario



Read_block and cycle processing

RESULTS

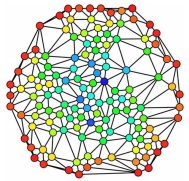
Algorithm	CPU latency	FPGA latency
Fast	4413000 **us**	98 **us**

Comparison of CPU latency and FPGA latency

Betweeness

INTRODUCTION

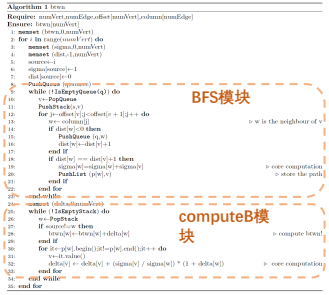
In graph theory, Betweenness Centrality is one of the measures of network graph centrality based on the shortest path. For a fully connected network diagram, any two nodes have at least one shortest path. The shortest path in an unweighted network diagram is the sum of the number of edges the path contains. The medial centrality of each node is the number of times these shortest paths pass through that node.



Betweenness Centrality in graph theory

CREATIVE DESIGN

The global algorithm can be divided into 2 main parts, BFS (Breadth First Search) module and ComputeB (Compute Betweenness Centrality) module, which could depend on latency of one cycle. Try to reduce latency by such methods: (1) Array splitting is used to increase read and write ports to achieve parallel processing (2) Reduction of pre-read data (3)Ensure that the pipeline input data interval is 1.



Algorithm structure of BC

RESULTS

Algorithm	CPU latency	FPGA latency
Betweenness	17.3 s	1.365 s

Comparison of CPU latency and FPGA latency