Research and FPGA Implementation of RDMA NIC Performance Enhancement

INTRODUCTION

High-performance computing requirements for networks lies on high throughput and low latency. The industry generally adopts RDMA (Remote Direct Memory Access) to replace the TCP protocol to achieve low latency and reduce the utilization rate of CPU of HPC server. Problems faced by commercial RDMA network cards: 1) adopt a DRAM-free design, and the network throughput decreases significantly when the number of QP connections increases. 2) lack one-to-many efficient and reliable communication support. The point-to-point RDMA RC protocol will introduce huge communication overhead in one-tomany/many-to-many scenarios



HPC with demand of high throughput and low latency



Data flow in RDMA system



Overview of design in system (WQE, AXI4-Lite, QDMA...)

Referring to the AMD OpenNIC Project, PCIe IP adopts QDMA and the network port adopts **100G CMAC**

1) Complete FPGA **RTL** process development, support standard network card and **RoCE v2 RC** some functions; The driver supports Linux kernel, compatible with **OFED API**, and supports perftest;

2) Efficient **WQE** Cache and prefetch mechanism implementation under Memory-free architecture (DRAM-free);

3) Based on **QDMA** multi-mode to realize various types of data interaction between the host and the board;

4) RDMA one-to-many reliable protocol design and implementation (WIP)

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On board test by Alveo U280





Illustrations of devices for compatibility test(upper and left) and end-to-end test(lower and right) respectively





 Table of performance in compatibility and end-to-end test

 (PMTU, Bandwidth Test, CPU Usage, Delay)

	PMTU	带宽测试 (Gbps)	CPU占用 (%)	发送1M数据的 时延(us)
兼容性测试	1024	89.37	6.25	121.89
端到端测试	1024	92.47	6.29	128.63