Hardware Accelerator Design and FPGA Implementation of Drug Docking Algorithm

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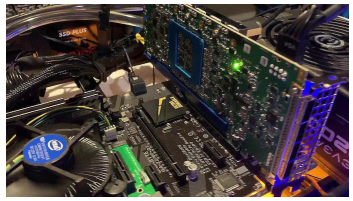
OpenHW2022

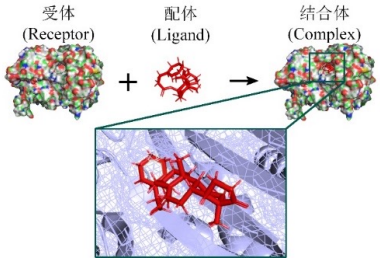
AMD XILINX



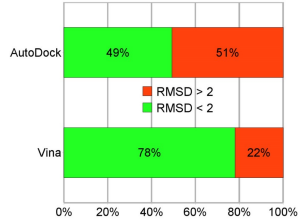
On board test by XCKU060

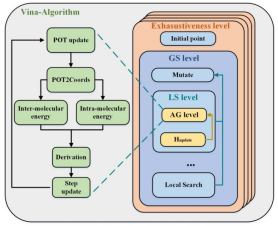
INTRODUCTION

Molecular docking (MD) is one of the core steps in the expensive and time-consuming process of drug design, which is basically an optimization problem based on scoring functions. **AutoDock Vina (Vina)** is the latest and most popular version due to its accuracy and relatively high speed, but hardware acceleration approaches of Vina are rarely reported. we propose **Vina-field programmable gate array (FPGA)**, a hardware-accelerated Vina implementation with FPGA that exploits the low-level parallelism.

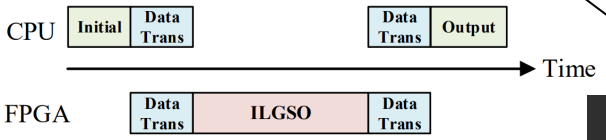


Drug design and popular software

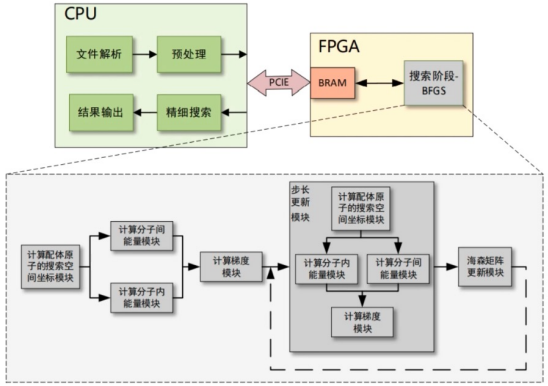




Data flow between CPU and FPGA



Set of multiple in-module hardware pipelines and BRAM

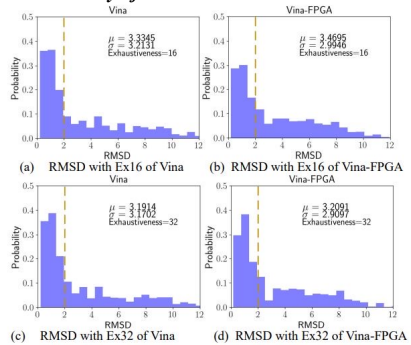


First, **the fixed-point quantization** is analyzed and realized to accelerate the MD algorithm with a better energy efficiency in hardware. To boost the performance of the module-level computation, **multiple in-module hardware pipelines** have been designed and implemented. Besides, a strategy for fast accessing to **block RAM (BRAM)** is implemented by **utilizing the layout of data**, which brings four times memory access speed to the intermolecular and intramolecular energy computing modules.

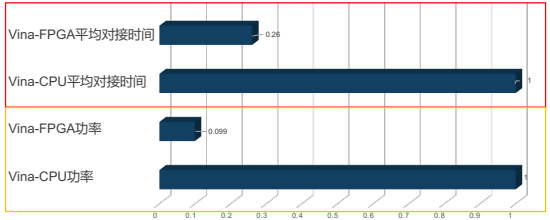
CREATIVE DESING

RESULT

Accuracy of Vina-FPGA and Vina



Under the same 140 ligand–receptor benchmarks, Vina-FPGA performs **up to 6.9× (average 3.7×) faster** than a state-of-the-art CPU does while **consuming only 2.5%** energy with similar docking accuracies. Compared to the GPU-accelerated implementation or Vina-GPU, the average **energy consumption of Vina-FPGA is merely 45%.**



Time and energy consumed by Vina-FPGA and Vina-CPU